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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,092	09/08/2003	Satoshi Kitamura	SIC-03-035	2091

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EXAMINER	
PARRIES, DRU M	
ART UNIT	**PAPER NUMBER**
2836	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/29/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/605,092	KITAMURA ET AL.	
	Examiner	Art Unit	
	Dru M. Parries	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed November 8, 2006 have been fully considered but they are not persuasive. Regarding the motivation to combine Turner and Nakabayashi, Turner teaches all of the components being powered by one battery pack with one single output voltage, and Nakabayashi teaches each component being powered by its own power storage element. Each load being powered by its own storage element, allows each load to receive a specified voltage corresponding to the amount of power needed by each specific load. Because all loads don't have the same power demand, having a storage element for each load will allow for a more precise voltage being supplied to each load individually, and therefore make the system more efficient with less power losses. This is also the explanation to the arguments regarding claim 24.

2. Regarding claims 2 and 3, Nakabayashi teaches a power-inhibiting unit (11) that "limits charging current" from the first to the second storage element. The power-inhibiting unit could also consist of switching means (14) and diodes (15).

3. Regarding claim 5, since Nakabayashi's storage element distribution system (and structure) is being implemented into Turner's invention, it would be obvious to use ALL of Nakabayashi's system (including reverse current inhibiting units) to prevent the current from flowing into areas of the Nakabayashi's system where it wasn't intended to flow. The fact that Turner doesn't acknowledge stray currents existing is moot, since the distribution system is being modified with Nakabayashi's plurality of storage elements, where the stray currents are more likely to be a problem.

4. Regarding claim 10, it would be obvious to have the first electrical component having a higher capacitance than the second electrical component, since it isn't specified what components correspond to which storage elements and since it has been held that rearranging parts (i.e. storage elements to corresponding electrical components) of an invention involves only routine skill in the art. *In re Japikse*, 86 USPQ 70.

5. Applicant's arguments with respect to claim 29 have been considered but are moot in view of the new ground(s) of rejection.

6. Regarding the obviousness of the modification using the Yoshimi reference, Yoshimi teaches a plurality of input voltage sources and corresponding switches to control the supply of power from each input to a particular part of the system, and using diodes, between the switches and the particular part of the system, to make sure the current doesn't flow back in the opposite direction towards the switch. Also, Nakabayashi teaches putting diodes in between a switch and an energy storage element. Both the Nakabayashi and Yoshimi references teach the use of diodes to prevent reverse flow of current. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to place diodes in between switches and storage elements to prevent the reverse flow of current.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-7 and 9-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Turner (2002/0014366) and Nakabayashi et al. (JP 04-150729 A). Turner teaches a bicycle power supply comprising an AC power supply (172) supplying power to a variety of electrical components (160-168; 174-184) through a plurality of batteries (170). He also teaches a rectifier (154) that converts the AC power to DC current to supply power to the plurality of storage elements. He also teaches some of the electrical components to be a mechanical adjusting mechanism (166, 168) (i.e. transmission or suspension), a microprocessor (150) and a sensor element (184) where the mechanical adjusting mechanism has a higher capacitance than the microprocessor. Turner fails to teach separate storage elements providing power to separate electrical components and a unit that prevents power flow from one storage element to another. Nakabayashi teaches two different storage elements (1st - 7 and 2nd - 12, 13) in parallel each structured to supply power to its own electrical component (10 and 16). He also teaches a power-inhibiting unit (11) to prevent power flow from the first storage element to the second component and from the second storage element to the first component. He also teaches reverse current inhibiting unit (15) coupled between the first and second storage elements to inhibit flow from the second storage element to the first. He also teaches preserving power in the first storage element when current is drawn from the second storage element to the second voltage system (16). He also teaches that current flows from the first storage element to the second via the reverse current inhibiting unit. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the plurality of batteries to supply power to their own individual loads (i.e. the first storage element supplying power to the mechanical adjusting mechanism and the second storage element supplying power to the microprocessor and/or a

sensor element) to be able to supply precise output values to each component in the system thereby creating a more efficient system. It also would have been obvious to one of ordinary skill in the art at the time of the invention to use the power and reverse current inhibiting units to eliminate stray currents that may cause malfunction in the system. None of the references explicitly teach which storage elements supply power to which electrical component, however, it would be obvious to pair any particular electrical component with any particular storage element since it has been held that rearranging parts (i.e. storage elements to corresponding electrical components) of an invention involves only routine skill in the art. *In re Japikse*, 86 USPQ 70.

9. Claims 8, 16-19, 22-25, 27-28, 31-32, and 34-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Turner (2002/0014366) and Nakabayashi et al. (JP 04-150729 A) as applied to claims 1 and 4-7 above, and further in view of Mitchell (6,355,990). Turner and Nakabayashi teach a bicycle power supply system as described above. They fail to teach a power switch unit that selectively switches current to a storage element in response to the voltage at that storage element and a voltage stabilizing circuit. Mitchell teaches a power switch unit (S1, S2, S3….Sn) that selectively switches current to the first split first storage element (C1) via switch (S1) and second split first storage element (C2) via switch (S2) in response to a voltage measured at the respective storage element. Mitchell teaches an unlimited amount of switches and storage elements (i.e. a first split second and second split second storage elements) for the plurality of loads that all work the same way as C1, C2, S1, and S2. The power switch unit is used to stabilize the voltage. It would have been obvious to one of ordinary skill in the art at the time of the invention to implement the power switches of Mitchell's invention into Turner's

system so that each storage element will have the right amount of stored voltage to power each individual load.

10. Claims 14, 15, 20, 21, 26, and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Turner (2002/0014366), Nakabayashi et al. (JP 04-150729 A), and Mitchell (6,355,990) as applied to claims 1, 4, 5, 13, 16, 19, 23-25, 31 and 32 above, and further in view of Yoshimi (JP 01-318519 A). Turner, Nakabayashi, and Mitchell teach a bicycle power supply as described above. They all fail to teach diodes between the power switch unit and each storage element. Yoshimi teaches reverse current inhibiting diodes (3-1, 3-2,….3-n) between switches (2-1, 2-2,…2-n), connected to an input, and an output. It would have been obvious to one of ordinary skill in the art at the time of the invention to place reverse current inhibiting diodes between the power switches and the storage elements so that no stray current will flow backward in the system when trying to charge the storage elements and possibly cause malfunction or incorrect voltages in other storage elements or electrical components.

11. Claims 29-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Turner (2002/0014366), Nakabayashi et al. (JP 04-150729 A), and Mitchell (6,355,990) as applied to claims 1 and 4, 5, 13, 16, 23-25, and 28 above, and further in view of Kitamura (2002/0128106). Turner, Nakabayashi, and Mitchell teach a bicycle power supply system as described above. Turner also teaches some electrical components being a transmission adjusting mechanism, and a microprocessor. They fail to teach an electrical component to be a suspension adjusting mechanism. Kitamura teaches a bicycle with an electrical component being a suspension

adjusting mechanism ([0081]). It would have been obvious to one of ordinary skill in the art at the time of the invention to have an electrical component in Turner to be the suspension adjusting mechanism of Kitamura so that the bicycle will be more versatile and add another feature to the bicycle. This will also make the bicycle ride more comfortably.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dru M. Parries whose telephone number is (571) 272-8542. The examiner can normally be reached on M-Th from 9:00am to 6:00pm. The examiner can also be reached on alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus, can be reached on 571-272-2800 x36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DMP

1-19-2007

CHAU N. NGUYEN
PRIMARY EXAMINER